

IN THE SPECIFICATION:

Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date) please enter the substitute specification in clean form and including paragraph numbers [0001] through [0083] and Abstract attached hereto as Appendix A. A marked-up substitute specification to clearly identify amendments to the specification as required by 37 C.F.R. § 1.121(b)(3)(iii) is attached hereto as Appendix B.

IN THE CLAIMS:

Claims 1, 3-5, 7-10, 12, 13, 17-25, 31, 33, 34, 38-45, 47, 49-57, 59-65, 67, 68, and 71-94 have been amended herein. All of the pending claims 1 through 94 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form in Appendix C attached hereto. Please enter these claims as amended. Also attached as Appendix D is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

IN THE DRAWINGS:

Also enclosed is a Transmittal of Formal Drawings with formal drawings revised as proposed.

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APPLICATION FOR LETTERS PATENT

for

**STACKED MASS STORAGE  
FLASH MEMORY PACKAGE**

Inventors:

Leonard E. Mess

Mike Brooks

David J. Corisis

Attorney:

James R. Duzan

Registration No. 28,393

TRASKBRITT

P.O. Box 2550

Salt Lake City, Utah 84110

(801) 532-1922

# STACKED MASS STORAGE FLASH MEMORY PACKAGE

## BACKGROUND OF THE INVENTION

[0001] Field of the Invention: This invention relates generally to packaged semiconductor devices. More particularly, the invention pertains to flash memory devices having high memory density.

[0002] State of the Art: The use of semiconductor integrated circuit (IC) chips is widespread, in both commercial grade and specific high reliability applications. Continuing progress in the manufacture of IC chips has resulted in chips of greatly increased density, i.e., higher [numbers]number of devices per footprint area of each chip. In addition, to produce increasingly complex electronic components, it is necessary to include a much greater number of IC chips on a substrate, e.g., a circuit board. One solution to this dilemma is to form a stack of chips on a substrate, creating what is known in the art as a multi-chip package.

[0003] The state of the art in vertically stacked multi-chip module (MCM) devices is illustrated by representative prior art devices shown in drawing FIGS. 1 through 11.

[0004] A representative example of a known multi-chip [semi-conductor]semiconductor apparatus 10, prior to packaging, is shown in drawing FIG. 1.

[0005] A plurality of chips or dice 12A, 12B and 12C are mounted in a pyramidal stack on a substrate 14. Each die is mounted with an adhesive material 16 to the next lower die or substrate[,] and is electrically connected to the metallized substrate 14 by bond wires 18 using known wire bonding methods. Variants of this multi-chip configuration are described in United States Patent 5,422,435 to Takiar et al., Japan Patent 62-8534(A) to Tsukahara and Japan Patent 3-165550(A) to Yashiro. In each of these references, a pyramidal stack is formed of increasingly smaller chips or dice 12, in order to accommodate the placement of bond wires 18 on peripheral portions of each die 12. This configuration is not generally useful where dice of equal dimensions are to be placed in a multi-chip module (MCM), such as in a memory device.

[0006] In drawing FIG. 2, a pyramidal stack of chips in device 10 is shown as described in United States Patent 5,399,898 to Rostoker. In these references, the dice 12A, 12B, 12C

comprise "flip-chips" with solder bumps or balls 20 joined to conductive areas on the backside 22 of the underlying chip.

[0007] Depicted in drawing FIG. 3 is a MCM configuration 10 in which a first die 12A is attached to a substrate 14 with adhesive 16[,] and is electrically connected to the substrate 14 with bond wires 18. A second die 12B is stacked atop the first die 12A and connected to it by solder balls 20. The second die 12B is smaller than the first die 12A, in order to leave access to the first die's 12A conductive areas. This type of arrangement is depicted in Japan Patent 56-158467(A) to Tsubouchi, and a variant thereof is described in Japan Patent 63-104343 to Kuranaga.

[0008] Depicted in drawing FIG. 4 is an MCM device 10 formed of dice 12A and 12D mounted on opposite surfaces of a substrate 14. In this example, the substrate 14 is a lead frame, and the construction permits both of the dice 12A, 12D to be connected to a metallization on one surface of the lead frame. This construction is described in United States Patent 5,012,323 to Farnworth.

[0009] Each of the above stacking configurations requires that the dice be of differing sizes. This is mandated by the need to leave the bond pads of each die unobstructed for wire attachment.

[0010] There have been various configurations of MCM packages in which chips of equal dimensions are stacked. Several such configurations are shown in drawing FIGS. 5, 6, 7, 8, 9, 10 and 11 and described below.

[0011] In one MCM configuration shown in United States Patent 5,973,403 to Wark and Japan Patent 5-13665(A) to Yamauchi, a flip-chip 12A is electrically bonded to a substrate 14 by posts, balls or other connectors 20, and a second chip, i.e., die 12B, is attached back-to-back to the flip-chip 12A (with an intervening insulation layer 24) and connected by wires 18 to the substrate 14. This particular MCM device 10 is illustrated in drawing FIG. 5.

[0012] In another form[,] depicted in drawing FIG. 6, two chips 12A, 12B are mounted on opposite sides of a substrate 14, with intervening insulation layers 24. The dice 12A, 12B are shown with [wire bonds]bond wires 18. This general dice-to-substrate configuration with variants

is pictured in United States Patent 5,147,815 to Casto, United States Patent 5,689,135 to Ball, and United States Patent 5,899,705 to Akram.

[0013] An MCM apparatus 10 which combines various die configurations already described above in drawing FIGS. 1 through 6 is shown in United States Patent 6,051,878 to Akram et al. The apparatus uses conductive column-like structures to connect substrates which carry the dice.

[0014] As shown in drawing FIG. 7, an MCM device 10 described in United States Patent 5,483,024 to Russell et al. has two identical dice 12A, 12B with central bond pads. The dice are sandwiched between and attached to two lead frames 14A, 14B with discontinuous adhesive layers 16. The dice 12A, 12B are joined by an intervening insulation layer 24. Bond wires 18 connect each die to the corresponding lead frame.

[0015] In drawing FIG. 8, a stacked MCM device 10 is depicted in accordance with the disclosure of United States Patent 5,323,060 to Fogal et al. In this device, dice 12A, 12B, 12C, and 12D are vertically alternated with adhesive layers 16A, 16B and 16C. The thickness of the adhesive layers is enhanced to be greater than the bond wire loop height, so that bond wires 18 may be attached to the active surfaces of the dice, for connection to the substrate 14.

[0016] Described in United States Patent 5,291,061 to Ball is a similar stacked device 10 in which the thickness of the adhesive layers 16A, 16B and 16C is reduced, using a low-loop-profile wire-bonding operation.

[0017] As shown in drawing FIG. 9, a configuration generally shown in United States Patent 5,399,898 to Rostoker uses an upper flip-chip die 12E to join dice 12A mounted on a substrate 14. The dice 12A are connected to substrate metallization with bond wires 18. Thus, the apparatus 10 comprises three dice connected serially.

[0018] There are various forms of a MCM apparatus in which separate enclosed units are first formed and then stacked. Examples are described in United States Patent 5,434,745 to Shokrgozar et al. and United States Patent 5,128,831 to Fox, III et al. A typical stacked apparatus 10 of this construction is depicted in drawing FIG. 10, showing three units. Each unit comprises an intermediate substrate 14A with a metallized surface. A die 12A, 12B or 12C is mounted on the intermediate substrate 14A[,] and connected to the metallization 30 by bond

wires 18. A wall 32 surrounding each die 12 encloses the die 12, bond wires 18, and metallization 30. The various metallization leads extend to conductive columns 34 within the wall 32, the latter connected to metallization 40 on substrate 14. An insulative cover 38 protects the upper unit and forms a protective shell about the device.

[0019] In another MCM package design 10 shown in drawing FIG. 11, a plurality of dice 12A, 12B,... have bevelled edges 28 which permit the bonding of wires to edge bond pads on the active surfaces 26. This design requires that the die thickness 36 be sufficiently great to accommodate wire loop height in the bevelled regions. If the die thickness 36 is insufficient, the thickness of adhesive layers 16 must be increased. Thus, the device height will be increased. Also, the bevelled[ die] edges 28 are weak and subject to breakage.

[0020] In each of the above prior art configurations for forming MCM packages containing a stack of identically configured dice, various limitations and/or problems exist as indicated above. A new package design is needed in which a plurality of identical dice with bond pads along one edge or two edges may be readily stacked for parallel operation. The new design must provide a package requiring fewer manufacturing steps and providing high density with enhanced reliability.

### BRIEF SUMMARY OF THE INVENTION

[0021] In accordance with the invention, a stacked multiple chip device is formed of two or more chips, i.e., dice, in which bond pads are located in areas along one or two edges of the active surface of each die. The device of the invention is particularly useful when configured to be formed of a stack of semiconductor dice which are substantially the same or similar in shape, size and bond pad arrangement, although not necessarily of identical shape, size and bond pad arrangement. An example of this die configuration is a mass memory storage device with a row or rows of bond pads along one edge of the semiconductor die.

[0022] In a device of this invention, the dice are arranged in a stack in which each individual semiconductor die being positionally offset from the next lower semiconductor die, thus exposing the bond pads of each die for wire bonding or other conductor attachment. In some embodiments, a semiconductor die may overhang bond pads of an underlying semiconductor die,

but the thickness of an intervening offset semiconductor die supporting the overhanging semiconductor die, together with two thin adhesive layers, provides sufficient "headroom" to accommodate the wire loop height. The thickness (Z-dimension) of adhesive layers may be minimized to reduce overall device height. Where bond pads are overhung by another die, wire bonding is successfully accomplished without the use of thick adhesive layers.

**[0023]** The substrate may be any body which supports the device, including for example, a circuit board, circuit card such as a multiple memory card, a lead frame or a tape automated bonding (TAB) tape. The bond pads of each die are exposed for rapid precise bond wiring to the substrate. In one embodiment, the apparatus is formed as a single stack of dice connected to a substrate whose reverse surface is configured for solder-ball bonding to another metallized surface.

**[0024]** In this invention, semiconductor dice having bond pads along one edge only need not be offset from each other in more than one direction. Semiconductor dice configured with bond pads along two adjacent edges are always offset from each other along two axes, i.e. in two directions. The offset exposes bond pads of a lower die to permit convenient wire bonding between each chip and a substrate.

**[0025]** Where the stack comprises more than two semiconductor dice, the offset of each semiconductor die may be positive or negative along both axes. The stack may include a reversal in the direction of offset. In this case, the die underlying the die having an offset direction change must also be rotated in orientation about a central Z-axis. The active surface of the semiconductor die may be rotated to place the bond pads adjacent a different location of the substrate. Such rotation may comprise 0, 90, 180 or 270 degrees in a clockwise or counter-clockwise direction.

**[0026]** Packaging of the device may use conventional processes for enclosing the semiconductor dice and conductors in a plastic, metal or ceramic encapsulant.

**[0027]** Some embodiments of the invention having up to four or more semiconductor dice provide complete exposure of all bond pads.

**[0028]** Use of this design provides adequate space for wire-bonding the bond pads which underlie die edges of a higher semiconductor die, because the spacer consists not of a thick

adhesive layer, but an intervening die or a piece of silicon or similar material substantially the same size as the semiconductor die. In some instances, inoperative semiconductor die may be used in the stack between operative semiconductor die located on either side thereof. The designs of the stack and the substrate are coordinated to provide an easily formed device which may for example have a high memory density, minimal height, short bond wires, small footprint, and high speed and responsiveness. In one embodiment, the package is particularly useful as a high speed multi-die mass storage flash memory device with a high memory density.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0029]** FIGS. 1 through 11 are side views of various prior art configurations of multi-chip modules (MCM);

**[0030]** FIG. 12 is an isometric view of an offset stacked multiple die device with a single offset in accordance with the invention;

**[0031]** FIG. 12A is an isometric view of an offset stacked multiple die device with a single offset, mounted on a lead frame, in accordance with the invention;

**[0032]** FIG. 12B is an isometric view of an offset stacked multiple die device with a single offset die of smaller size, mounted on a lead frame, in accordance with the invention;

**[0033]** FIG. 12C is an isometric view of an offset stacked multiple die device with a single offset die of larger size, mounted on a lead frame, in accordance with the invention;

**[0034]** FIG. 13 is a side view of an offset stacked multiple die device with a single offset in accordance with the invention;

**[0035]** FIG. 14 is a plan view of an offset stacked multiple die device with a single offset in accordance with the invention;

**[0036]** FIG. 15 is a side view of another embodiment of an offset stacked multiple die device in accordance with the invention;

**[0037]** FIG. 16 is a side view of a further embodiment of an offset stacked multiple die device in accordance with the invention;



[0038] FIGS. 17 through 24 are simplified side views of various exemplary embodiments of unencapsulated stacked multiple die devices having different configurations of one-axis die stacking and wire bonding, in which:

[0039] FIG. 17 is a side view of an offset stacked multiple die device having forwardly offset dice connected to a substrate, in accordance with the invention;

[0040] FIG. 18 is a side view of another embodiment of an offset stacked multiple die device having forwardly offset dice connected to a substrate, in accordance with the invention;

[0041] FIG. 19 is a side view of an offset stacked multiple die device having one rearwardly offset die and two forwardly offset dice connected to a substrate, in accordance with the invention;

[0042] FIG. 20 is a side view of another embodiment of an offset stacked multiple die device having one rearwardly offset die and two forwardly offset dice connected to a substrate, in accordance with the invention;

[0043] FIG. 21 is a side view of an offset stacked multiple die device having two rearwardly offset dice and one forwardly offset die connected to a substrate, in accordance with the invention;

[0044] FIG. 22 is a side view of another embodiment of an offset stacked multiple die device having two rearwardly offset dice and one forwardly offset die connected to a substrate, in accordance with the invention;

[0045] FIG. 23 is a side view of an offset stacked multiple die device having four dice with alternating forward and rearward offset, connected to a substrate, in accordance with the invention;

[0046] FIG. 24 is a side view of another embodiment of an offset stacked multiple die device having four dice with alternating forward and rearward offset, connected to a substrate, in accordance with the invention;

[0047] FIG. 25 is a side view of another embodiment of an offset stacked multiple die device having four dice which are sequentially rotated and offset in at least one direction;

[0048] FIG. 26 is a plan view of an embodiment of an offset stacked multiple die device having four dice which are sequentially rotated and offset in at least one direction, in accordance with the invention;

[0049] FIG. 27 is an isometric view of an offset stacked multiple die device formed of two dice with bond pads along two adjacent edges wherein an upper die is offset from an underlying die along both the X-axis and Y-axis in accordance with the invention;

[0050] FIG. 28 is a side view of an offset stacked multiple die device formed of four [elongate]elongated dice which have bond pads along two opposing edges wherein dice are arranged in an alternating sequence providing an offset from all dice, in accordance with the invention; and

[0051] FIG. 29 is a plan view of an offset stacked multiple die device formed of four [elongate]elongated dice which have bond pads along two opposing edges wherein dice are arranged in an alternating sequence providing an offset from all dice, in accordance with the invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0052] A new stacked multiple chip device formed of a plurality of offset Z-stacked, i.e., vertically-stacked semiconductor dice, together with a method of production thereof[,] are provided by the invention. Some devices of the invention may be classified as stacked multi-chip modules (MCM). Semiconductor dice which are particularly usefully stacked in this construction are those having conductive bond pads along one edge, or alternatively along two adjacent edges of the active surface. In addition, a particular embodiment will be described which utilizes [elongate]elongated, i.e., semiconductor dice having bond pads along opposing distal edges of a [non-square elongate]nonsquare elongated active surface. Although the device is particularly adapted to dice of the same surface dimensions and similar bond pad layout, a stack of dice may be formed in accordance with this invention which includes one or more semiconductor dice of a differing configuration at either end of the stack, or interposed therein. The stack of semiconductor dice is physically attached to a substrate, in which the substrate may comprise, for example, a printed circuit board (PCB), a memory card, a lead frame, tape automated bonding

(TAB) tape or other substrate. Additionally, similar shaped dummy die of silicon and the like may be used as spacers between semiconductor die in the stack.

[0053] In the figures and this description, semiconductor dice and any spacers in general will be denoted by the numeral 60, and a letter suffix i.e. A, B, C, etc. will be used to identify a particular semiconductor die or spacer or the like of a stack. Numerals identifying bond pads, bond wires, etc. which relate to a particular semiconductor die will carry the same suffix.

[0054] In this description, bond wires will be described as being connected between a semiconductor die and a substrate. It is to be understood that the wires are bonded to bond pads on the semiconductor die and to conductive members such as metallization or a lead frame which may constitute all or part of the substrate. The device may also include semiconductor die-to-semiconductor die bonds.

[0055] With reference to the drawings of drawing FIGS. 12, 13 and 14, which describe an embodiment of the instant invention, a semiconductor device 50 having a multi-chip module (MCM) type of configuration comprises two semiconductor dice 60A and 60B as a stack 61. This configuration is particularly appropriate to flash memory packages in which the die circuits are connected in parallel. In this configuration, the semiconductor dice 60A, 60B have essentially identical circuits[,] and have upwardly facing active surfaces 52A, 52B with bond pads 54A, 54B along one edge 56A, 56B of each active surface, respectively. The bond pads of each semiconductor die 60 are collectively designated as a "field" 55 of bond pads. Each semiconductor die 60A, 60B has a length dimension 104 and a width dimension 106 which may be equal or unequal thereby making the die 60A, 60B have different physical sizes and shapes.

[0056] Semiconductor die 60A is shown attached to a substrate 70 by adhesive layer 78. The adhesive layer 78 may be any adhesive capable of bonding a reverse surface 72 of a die 60 to the active surface 52 of another semiconductor die or to a topside 66 of a substrate 70. Semiconductor die 60B is stacked on top of semiconductor die 60A and joined to it by thin adhesive layer 78. Semiconductor die 60B is offset from semiconductor die 60A along Y-axis 76 a distance 82 which exposes the field 55 of bond pads 54A. The offset distance 82 may be the shortest distance which permits reliable use of a wire bonding tool, not shown, to bond conductors such as bond wires 62 to the bond pads 54A. Thus, bond pads 54A, 54B are joined

by fine metal bond wires 62 or other conductive members to conductive, e.g., metallization areas 58 on the topside 66 of substrate 70. If so dictated by the design of the device 50, certain bond pads 54A and 54B may also be conductively connected to each other, i.e., on the same semiconductor die 60A or 60B, or from semiconductor die 60A to semiconductor die 60B.

[0057] In these figures, the substrate 70 is pictured as a circuit board or memory card substrate or multimedia card substrate, for example. This example is shown with solder balls 64 on its reverse side 68 although other configurations of electrical connections may be used.

[0058] A controlled thickness thermoplastic or other type of adhesive may be used in adhesive layers 78 to join the semiconductor dice 60A and 60B to each other, and semiconductor die 60A to the substrate 70.

[0059] The bond pads 54A and 54B of dice 60A and 60B, respectively, are joined to metallization or other [conductors]conductive areas 58 on the substrate 70 by thin bond wires 62. Typically, the bond wires 62 have a diameter of about 0.001 inch[,] and are formed of a metal such as aluminum or gold, or alloys thereof. The preferred method of bonding the bond wires 62 to the bond pads is known as ultrasonic ball bonding, which forms a low-loop wire bond which is less than the Z-dimension of a semiconductor die 60. Likewise, in a preferred method, ultrasonic "wedge" bonds of wire are formed at the substrate metallization 58.

[0060] In general, semiconductor devices are encapsulated in a protective package to protect the die surfaces, metallization and wires from damage. As depicted in drawing FIGS. 12 through 14, edges of an exemplary equiangular encapsulating enclosure are defined by lines 84. The encapsulant material may be a polymer, ceramic or other protective material. As shown, the completed, i.e., packaged device 50 may be formed to have a low profile vertical (Z) dimension 86 (excluding solder balls 64) which is less than prior stacked device heights, because thick intervening layers of adhesive are not required between adjacent semiconductor dice 60.

[0061] A stack 61 of two or more offset semiconductor dice 60 may also be formed on a lead frame 94, as depicted in an example in drawing FIG. 12A. The lead frame 94 is typically formed from a material such as copper, copper alloys, iron-nickel alloys, or the like. Other materials, such as TAB tape, could be used in accordance with this invention as well. The lead frame 94 is shown with opposing runners 96, a central paddle 98, and leads 102 to which wires

are attached. The lead frame 94 has alignment mechanisms 100 such as precisely positioned marks or holes, for precise positioning of the lead frame 94 during operations such as die bonding and wire bonding where alignment is critical. In this example, semiconductor die 60A is attached to a paddle 98 of lead frame 94 with a thin adhesive layer, not shown. The paddle 98 serves as a substrate to support the stack 61. Semiconductor die 60B is then attached to overlie a major portion of semiconductor die 60A, wherein the die edge 56B along which bond pads 54 are positioned is offset a distance 82 from the die edge 56A of the lower semiconductor die 60A, to expose the bond pads 54. As shown, conductive bond wires 62A are connected from bond pads [56A]54B of semiconductor die 60A to appropriate leads 102A. Likewise, bond wires 62B are connected from bond pads 56B to leads 102B. Alternatively, TAB bonding or other bonding methods may be used. As illustrated in drawing FIG. 12B, the semiconductor die 60B is of smaller size than that of semiconductor die 60A. Further, as illustrated in drawing FIG. 12C, the semiconductor die 60B is of larger size than semiconductor die 60A having three sides of the semiconductor die 60B overhanging the semiconductor die 60A.

[0062] In the embodiment of drawing FIGS. 12 through 14, both of the semiconductor dice 60A, 60B have their bond pads 54A, 54B oriented in the same direction so that they are connected by bond wires 62 to metallization areas 58 on the same side of the device 50. However, the semiconductor die orientation and other factors, such as semiconductor die having different sizes and dimensions, may be changed to suit a particular application. Thus, major design factors affecting the stacked offset multiple semiconductor die device 50 include the number of semiconductor dice 60 in the stack 61, die dimensions, number of die edges 56 along which bond pads 54 are arrayed, offset direction(s), offset distance 82 and rotation angle of each semiconductor die 60 relative to the semiconductor die 60 just below.

[0063] As shown in drawing FIG. 15, semiconductor die 60B has been rotated 180 degrees about central Z-axis 88 such that its edge 56B along which bond pads 54B are positioned is opposite in direction to edge 56A of semiconductor die 60A. It is evident that semiconductor die 60B may alternatively be rotated zero degrees, 90 degrees, 180 degrees or 270 degrees relative to die semiconductor 60A. The conductive metallization 58 on the substrate 70 must be configured for providing short bond wire connections with the bond pads 54A, 54B.

**[0064]** Depicted in drawing FIG. 16 is an offset stacked 2-semiconductor die device 50 in which the upper semiconductor die 60B is rotated 90 degrees clockwise about Z-axis 88. Thus, the row(s) of bond pads 54B are rotated 90 degrees from the row(s) of bond pads 54A. In this embodiment, both semiconductor dice 60A, 60B are depicted as having active surfaces 26 which are substantially square but the device 50 may be formed of substantially [non-square]nonsquare semiconductor dice.

**[0065]** As will be evident, a variety of offset stacking configurations is available when using semiconductor dice 60 with bond pads 54 along one edge 56. Depicted in drawing FIGS. 17 through 24 is a variety of such configurations; this application is not limited to these particular configurations, which serve as examples. Each of these figures relates to a stack 61 of four offset semiconductor dice 60A, 60B, 60C and 60D in which individual semiconductor die may be offset in a forward direction, i.e., to the right, or in a reverse direction, i.e., to the left. In addition, an individual semiconductor die 60 may be rotated 180 degrees so that the bond pad location is reversed relative to the underlying semiconductor die. Reversal of a semiconductor die 60 results in attachment of its bond pads 54 to substrate 70 in a different location.

**[0066]** For the sake of clarity, drawing FIGS. 17 through 24 do not show adhesive layers, encapsulating material or other details of the device 50. The number of semiconductor dice 60 comprising the stack 61 is limited only by design, construction and operational limitations such as materials strength, heat generation and dissipation, electric operability and the like. The design of the stack 61 must be coordinated with substrate design, i.e., to ensure accurate and rapid wire bonding and meet other design criteria.

**[0067]** As shown in drawing FIG. 17, a plurality of semiconductor dice 60A, 60B, 60C and 60D may be consecutively stacked in a single offset direction, denoted herein as a "forward" direction. All of the semiconductor dice have bond pads 54 facing in the same direction. In this stacking configuration, the bond wires 62A, 62B, 62C or 62D of each semiconductor die is bonded to a substrate 70 at the same side of the stack 61.

**[0068]** The embodiment of drawing FIG. 18 differs from drawing FIG. 17 in that the uppermost semiconductor die 60D is rotated 180 degrees relative to the other semiconductor dice, and has bond pads 54D attached to the substrate 70 on the other side of the stack 61.

[0069] Illustrated in drawing FIGS. 19 through 24 are other offset multiple semiconductor die devices 50 in which semiconductor dice 60 are offset in both forward and reverse directions.

[0070] Illustrated in drawing FIGS. 19 and 20 are devices 50 which have a second semiconductor die 60B with a reverse offset and which is rotated 180 degrees relative to lowermost semiconductor die 60A. Semiconductor dice 60C and 60D are similarly rotated relative to semiconductor die 60A, and each is forwardly offset from its underlying die. In drawing FIG. 19, the bond wires 62 from the three upper semiconductor dice 60B, 60C and 60D are bonded to the substrate 70 on the same side of the stack 61, while semiconductor die 60A is bonded on the opposing side of the stack. In drawing FIG. 20, semiconductor die 60D is attached to the stack 61 in an unrotated position relative to die 60A. Semiconductor die 60D has its bond wires 62D connected to substrate 14 in the vicinity of bond wires 62A, i.e., on the opposite side of the stack from bond wires 62B and 62C.

[0071] As illustrated in drawing FIGS. 21 and 22, semiconductor dice 60B and 60C are offset in a reverse direction from semiconductor die 60A, and semiconductor die 60D is offset in a positive direction from underlying die 60C. Illustrated in drawing FIG. 21, semiconductor dice 60C and 60D are both rotated 180 degrees relative to semiconductor dice 60A and 60B, so that their bond pads 54C and 54D face in an opposite direction from bond pads 54A and 54B. Illustrated in drawing FIG. 22, semiconductor die 60D of the device 50 in drawing FIG. 21 has been rotated 180 degrees and its bond wires 62D attached to the substrate 14 in the vicinity of bond wires 62A and 62B.

[0072] As shown in drawing FIG. 23, the semiconductor dice 60 in stack 61 may be ordered in an alternating fashion with respect to both die rotation, i.e., between a forward and reverse direction, and offset direction.

[0073] Alternatively, as shown in drawing FIG. 24, the uppermost semiconductor die 60D of a stack may have the same alternating offset pattern as the device 50 of drawing FIG. 23, but be rotated to have the same rotational orientation as its underlying semiconductor die 60C. The bond wires 62D will be joined to the substrate 70 in the vicinity of bond wires 62A and 62C.

[0074] Where the bond pads 54 of a die 60 are overhung by a portion of another semiconductor die, those bond pads may be wire-bonded to the substrate 70 prior to mounting the overhanging die in the stack 61. Using the configuration illustrated in drawing FIG. 19 as an example, it is seen that bond pads 54A are overhung by a portion of semiconductor die 60C. The height 92 of wire loop 90 is less than the die thickness 36, enabling wire bonding without subsequent contact of bond wires 62 with the overhanging semiconductor die 60C or intervening semiconductor die 60B or silicon spacer 60B.

[0075] Turning now to drawing FIGS. 25 and 26, another embodiment of an offset stacked device 50 is shown with a stack 61 of four semiconductor dice 60A, 60B, 60C and 60D. Each semiconductor die 60 has a square active surface 52 and all semiconductor dice 60 are constructed to be physically identical. By rotating each semiconductor die 60 to be 90 degrees from the next lower die, and offsetting each successive semiconductor die to avoid the bond pads 54 of the next lower semiconductor die, all bond pads 54 of the four semiconductor dice 60 are exposed for wire bonding in a single uninterrupted step.

[0076] The stacked offset multiple die device 50 of this invention may have any form of substrate 70 known in the art. For example, the substrate 70 may be a metallized lead frame as already shown in drawing FIG. 12A.

[0077] Turning now to drawing FIG. 27, yet another embodiment of an offset stacked device 50 of the invention is shown which is formed of two or more semiconductor dice such as semiconductor dice 60A, 60B having conductive bond pads 54A and 54B, respectively. The two semiconductor dice are joined together and to substrate 70 by thin adhesive layers 78. On each semiconductor die, the bond pads are shown as formed along two adjacent edges of the semiconductor die. Thus, for example, semiconductor die 60A has bond pads 54AA formed along die edge 56AA, and bond pads 54AB formed along adjacent die edge 56AB. Likewise, semiconductor die 60B has bond pads 54BA formed along die edge 56BB.

[0078] As shown in drawing FIG. 27, die 60B is offset in position in two directions. Thus, semiconductor die 60B is offset from semiconductor die 60A a distance 82A along the X-axis 74 and a distance 82B along the Y-axis 76, whereby all of the bond pads 54AA and 54AB of semiconductor die 60A are exposed for easy wire bonding.



[0079] Additional semiconductor dice 60 may be mounted atop semiconductor die 60B. These semiconductor dice may be mounted in the same sequence, using a substrate 70 configured with metallization on two sides only of the stack 61. Alternatively, subsequent semiconductor dice 60C,... may be mounted atop semiconductor die 60B having the same pattern of offset, i.e., along both the X-axis 74 and Y-axis 76, but rotated 180 degrees relative to semiconductor dice 60A and 60B. As a result, wire bonds will be made to the substrate 70 on four sides of stack 61.

[0080] A further embodiment of the invention is illustrated in drawing FIGS. 28 and 29, in which a semiconductor die stack 61 is formed of semiconductor dice 60 having bond pads 54 on each of two opposed edges 56 of the semiconductor die's active surface 52 (not shown). In this configuration, each added semiconductor die 60 is rotated 90 degrees or 270 degrees from the underlying semiconductor die to place the semiconductor die in an offset position. Each semiconductor die 60 has a length dimension 104 (not shown) which is longer than a width dimension 106 (not shown) by at least two times the required offset, i.e., to expose the bond pads 54 of the underlying semiconductor die. If desired, the semiconductor dice 60 can be of any convenient physical size and be of different physical size than the other. Use of more than two semiconductor dice 60 in the stack 61 results in semiconductor die pads 54 being overhung by a semiconductor die which is two positions higher in the stack. The manufacturing process will require intermediate wire bonding operations in this case. The stack configuration results in wire bonds 62A and 62C to metallization areas 58 of the substrate 70 on two opposing sides of the stack 61, and wire bonds 62B and 62D on the other two opposing sides of the stack. Thus, wire bonds are located on all four sides of the stack 61.

[0081] As described herein, the invention provides a stacked multiple semiconductor die device or package of higher electronic density, in which individual die of similar size, different size, or the same size are offset from each other in the stack, enabling electrical attachment, e.g., wire bonding between the semiconductor dice and a substrate. Thus, the overall height of the stack of semiconductor dice, and the package formed therefrom, is minimal. Multiples of the stacked multiple die package may be combined in a large mass storage flash memory apparatus, for example.

[0082] The various embodiments of stacked offset multiple semiconductor die devices which are shown and described herein are exemplary and not limiting. It is understood that other configurations may include additional elements, for example, such elements including additional semiconductor dice and lead frames, heatsinks, dielectric layers, packaging, etc., as known in the art.

[0083] It is apparent to those skilled in the art that various changes and modifications may be made in the packaging methods and products of the invention as disclosed herein without departing from the spirit and scope of the invention as defined in the following claims.